CLAIMS

1. A method of generating pulsed first and second switching signals for switching first and second switches of a switching circuit further comprising an output and that receives a DC signal of voltage $+V_S$, wherein switching between various combinations of on and off states of the first and second switches produces a voltage at the output with pulses at levels of $+V_S$, 0V and $-V_S$;

the method comprising the steps of:

(a) receiving a voltage demand signal indicative of a desired voltage to be supplied at the output in a period; and

(b) generating the first and second switching signals according to a first rule that the first switching signal shall have a single pulse of a first determined width within the period and, subject to a second rule that the pulse width of the resulting voltage at the output must not fall below a minimum pulse width, that the second switching signal shall remain in one state throughout the period; the first determined width being such that the combination of the first and second switching signals when applied to the first and second switches respectively produce an average voltage at the output for the period being substantially equal to the desired voltage.

2. The method of claim 1 comprising the step of generating the first and second switching signals according to a rule that pulse widths below the minimum pulse width are avoided by departing from the rule that the second switching signal shall remain in one state throughout a period in favour of a rule that the second switching signal shall have a single pulse of a second determined width within the period to create a voltage pulse at the output of either $+V_S$ or $-V_S$.

3. The method of claim 2 comprising the step of adding the second determined width to the first determined width such that the voltage pulse at the output of $+V_S$ or $-V_S$ resulting from the pulse in the second switching signal is balanced by an

equal width of voltage pulse at the output of $-V_S$ or $+V_S$ respectively resulting from the increased first determined width of the first switching signal.

4. The method of claims 2 or 3 comprising the step of generating the first and second switching signals according to a rule that the leading and trailing edges of the first switching signal do not coincide with either the leading or trailing edge of the second switching signal.

5. The method of any preceding claim comprising the step of generating the first and second switching signals according to a rule that any pulse should be positioned symmetrically about the centre of the period.

6. The method of claim 5 comprising the step of generating the first and second switching signals according to the rule that where pulses cannot be centred symmetrically, the longer and shorter sides of the asymmetric pulses are alternated between the leading edge side and the trailing edge side for successive asymmetric pulses.

7. The method of any preceding claim further comprising the step of noise shaping the first and second switching signals.

8. A method of operating a switching circuit comprising a bridge circuit having an input that receives a DC signal of voltage $+V_S$, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output,

the method comprising the steps of:

(a) generating pulsed first and second switching signals in accordance with any preceding claim; and

(b) supplying the first and second switching signals to the first and second switches respectively thereby to cause the first and second switches to switch between on and off states, switching between various combinations of on and off states producing an electrical signal across the output with voltage pulses at levels of $+V_S$, 0V and $-V_S$ and with an average voltage for the period substantially equal to the desired voltage.

9. The method of claim 8, wherein either the first or second determined pulse width is generated with reference to a voltage signal indicative of the DC signal such that the determined pulse width compensates for fluctuations in the DC supply.

10. The method of claim 9, wherein the voltage signal is passed through a filter to obtain a predictive measure of fluctuations in the DC supply.

11. The method of claim 10, wherein the voltage signal is passed through a finite impulse response filter.

12. The method of any of claims 8 to 11, wherein either the first or second determined pulse width is generated to include additional width to compensate for a voltage drop across a diode and/or transistor in the bridge circuit.

13. The method of claim 12, wherein the additional width is calculated with reference to a current signal indicative of the current flowing through the output and a representative resistance of the diode or transistor.

14. The method of any of claims 8 to 13, wherein the width of a pulse of the first or second switching signals is generated to include additional width to compensate for a voltage offset caused by slow response times in the first or second switch.

15. The method of any preceding claim, wherein the first and second switches are transistors and the method comprises the step of switching the transistors between on and off states corresponding to substantially maximum and substantially minimum current flow respectively through the transistors.

16. The method of any preceding claim comprising the step of receiving a current demand signal indicative of a desired current to be supplied to the output in a period and calculating the voltage demand signal indicative of a desired voltage to be supplied to the output that results in an electrical signal being supplied to the output during the period with a current substantially equal to the desired current.

17. The method of claim 16, wherein the step of calculating the voltage demand signal is performed with reference to a model of the load characteristic of a load connected to the output.

18. The method of claim 16 or claim 17 further comprising the step of generating the voltage demand signal with reference to a current signal indicative of the current flowing through the output.

19. A computer program comprising program code means for performing the method steps of any of claims 1 to 18 when the program is run on a computer and/or other processing means associated with the switching circuit.

20. A computer program product comprising program code means stored on a computer readable medium for performing the method steps of any of claims 1 to 18 when the program is run on a computer and/or other processing means associated with the switching circuit.

21. A switching circuit operable to receive a DC signal of voltage $+V_S$ and that comprises first and second switches, an output and processing means programmed to perform the method steps of any of claims 1 to 6.

22. A switching circuit according to claim 21, further comprising a noise shaper operable to noise shape the first and second switching signals.

23. A bridge circuit comprising an input operable to receive a DC signal of voltage $+V_S$, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output and processing means programmed to perform the method steps of any of claims 8, 14, 16 or 17.

24. A bridge circuit according to claim 23, further comprising voltage signal sensor operable to produce a voltage signal and wherein the processing means is programmed to perform the method steps of claim 9.

25. A bridge circuit according to claim 24, further comprising a filter arranged to receive the voltage signal.

26. A bridge circuit according to claim 25, wherein the filter is a finite impulse response filter.

27. A bridge circuit according to claim 26, further comprising a diode and/or transistor and wherein the processing means is programmed to perform the method steps of claims 12 or 15.

28. A bridge circuit according to claim 23 to 27, further comprising a current signal sensor operable to produce a current signal and wherein the processing means are programmed to perform the method steps of claims 13 or 18.

29 A method of generating pulsed first and second switching signals substantially as hereinbefore described with reference to any of Figures 1 to 6.

30 A method of operating a switching circuit substantially as hereinbefore described with reference to any of Figures 1 to 6.

31 A switching circuit substantially as hereinbefore described with reference to any of Figures 1 to 6.